MICRO-TRENCH OXIDATION BY USING ROUGH OXIDE MASK FOR FIELD ISOLATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the field of integrated circuits fabrication, and more particularly, to a process of forming local field oxide isolation regions without bird's beak.

2. Description of the Prior Art

In the conventional integrated circuits fabrication, isolation is achieved by either local oxidation (LOCOS) or shallow trench isolation (STI). However, both are suffered from the so-called bird's beak formation which is caused by oxygen encroachment into the active regions during the oxidation. Referring now to FIG. **1**, it illustrates a typical bird's beak region **14** at the areas where the field oxide **12** is adjacent to the active regions of the silicon substrate **10**. These bird's beak regions cause problems in subsequent processing particularly as the allowable dimensional tolerances of the integrated circuits become smaller.

Within the prior art, there are some references addressing the bird's beak issue, however, none appears to be directed to the specific application of the present invention, namely the use of rough oxide mask to form multiple trenches for smoother field oxide growth.

For example, U.S. Pat. No. 5,374,583 to Lur et al. (the entire disclosure of which is herein incorporated by reference) discloses the use of aluminum—silicon alloy mask to etch a set of narrow trenches. Another paper titled "Nano-Trenched Local Oxidation of Silicon Isolation Using Island Polysilicon Grains" by Kwon et al., J. Electrochem. Soc., Vol. 143, No. 2, pp. 639–642, 1996, teaches the use of island polysilicon grains (IPG) mask. But the processes are too complicated and the materials are not often used in a semiconductor factory to be practically employed for integrated circuits mass-production.

SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a method of forming local isolation in an integrated circuit.

It is another object of the present invention to provide a method of forming local isolation by using rough oxide as a mask to reduce or eliminate the bird's beak formation.

Yet, another object of the present invention is to provide an effective and manufacturable method to locally oxidize silicon substrate for isolation in an integrated circuit.

These objects are accomplished by the fabrication process described below.

First, a layer of first dielectric is formed on the surface of a monocrystalline silicon substrate. The first dielectric layer is then patterned to define active device region and isolation region by the conventional lithography and etching techniques. Next, a very thin layer of second dielectric is deposited over the entire silicon substrate surface, followed by depositing a layer of rough oxide with predetermined grain size overlaying the second dielectric layer. Next step is the key point of the present invention, by using rough oxide grains as an etching mask, the second dielectric layer and the silicon substrate underneath are spontaneously etched to form multiple trenches in the isolation region. Next, the rough oxide grains and second dielectric layers are stripped. Then, field oxidation is performed to form a smoother field oxide isolation region. The local field oxide isolation regions without bird's beak according to the present invention is finally accomplished.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings forming a material part of this description, in which:

FIG. **1** shows a cross sectional representation of a field oxide region with bird's beaks formed by a conventional LOCOS process.

FIG. **2** shows a cross sectional representation of a silicon substrate after the isolation region is defined according to the first embodiment of the present invention.

FIG. **3** shows a cross sectional representation of a silicon substrate after the rough oxide is formed according to the first embodiment of the present invention.

FIG. **4** shows a cross sectional representation of a silicon substrate after multiple trenches are formed according to the first embodiment of the present invention.

FIG. **5** shows a cross sectional representation of a silicon substrate after the isolation region without bird's beak is accomplished according to the present invention.

FIG. **6** shows a cross sectional representation of a silicon substrate after the rough oxide is formed according to the second embodiment of the present invention.

FIG. **7** shows a cross sectional representation of a silicon substrate after multiple trenches are formed according to the first embodiment of the present invention.

FIG. **8** illustrates the grain size of the rough oxide is a function of the ozone concentration according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention discloses herein is directed to a process of forming local field oxide isolation regions without bird's beak. The drawing figures are illustrated a partially completed silicon substrate. In the following description, numerous details are set forth in order to provide a thorough understanding of the present invention. It will be appreciated by one skilled in the art that variations of these specific details are possible while still achieving the results of the present invention. In other instance, well-known processing steps are not described in detail in order not to unnecessarily obscure the present invention.

Referring now more particularly to FIG. **2**, a layer of first dielectric **23** is formed on the surface of a monocrystalline silicon substrate **21**. The first dielectric layer **23** is then patterned to define active device region **25** and isolation region **27** by the conventional lithography and etching techniques.

The first dielectric layer **23** is thermally grown or chemically vapor deposited (CVD) silicon dioxide to a thickness of about 500 to 1000 Angstroms. Alternatively, the first dielectric layer **23** can be silicon nitride or silicon dioxide/silicon nitride double layers. The first dielectric layer etching process is using dry etching technique with CF_4, CHF_3 and O_2 reactant gases.

Referring now to FIG. **3**, a very thin layer of thermal oxide **29** which has a thickness of about 50 to 150 Angstroms is grown over the silicon substrate **21** surface in the isolation region **27**, followed by depositing a layer of rough oxide **31** with predetermined grain size over the entire silicon substrate surface.